REMARKS

This paper is responsive to an Office Action mailed July 13, 2005. Prior to this amendment, claims 17-48 were pending. After amending claims 17-18, 20-21, 33-36, and 38-39, claims 17-48 remain pending.

In Section 2 of the Office Action claims 17-48 have been rejected under 35 U.S.C. 112, second paragraph, as incomplete for omitting essential elements. With respect to claim 17, the Office Action states that the omitted element is the relationship between a "channel equalization communication system" and the body of the claims, citing MPEP 2172.01.

With respect to claim 35, the Office Action states that there is an omitted relationship between "non-causal channel equalization communication system" and the body of the claims.

With respect to claim 17, the Office Action states that there is no antecedent basis for "each NRZ data", and that the relationship between "each NRZ data" and a "NRZ data stream" is not clear.

With respect to claim 33, the Office Action states that there is no antecedent basis for "each data", and that the relationship between "each data" and a "data stream" is not clear.

With respect to claim 35, the Office Action states that there is no antecedent basis for "each data", and that the relationship between "each data" and a "data stream" is not clear.

With respect to claims 17, 33, and 35, the Office Action points out the difficulties of making a proper prior art search. The Office Action also states that a "communication system" includes a transmitter, but that the claims do not appear to be directed to a transmitter. This rejection is traversed as follows.

The second paragraph of 35 U.S.C. 112 states that "(t)he patent specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter of the invention."

MPEP 2171.01 states that, "a claim which fails to interrelate essential elements of the invention as defined by applicant(s) in the specification may be rejected under 35 U.S.C. 112, second paragraph, for failure to point out and distinctly claim the invention."

Neither of these cited passages discusses any particular relationship between the preamble and the claim elements. The claimed invention is a non-causal channel equalization system that, in its broadest expression, comprises two elements: a non-causal circuit and a multi-threshold circuit. The Applicant respectfully submits that is no ambiguity in reciting that a non-causal circuit is one of the elements of a non-causal equalization system. Alternately stated, the preamble presents a communications system. The description of the system as a non-causal channel equalization system creates a bridge to the non-causal circuit claim element.

In each of the Office Actions made against this application, rejections have been made under 35 U.S.C. 112, second paragraph. The Applicant has amended the claims on several occasions in response to these rejections. However, every claim amendment appears to simply lead to a new rejection. As noted above, the Office Action complains of the substantial burden required to perform an adequate prior art search. In retrospect, it appears to the Applicant that the purpose of the '112 rejections has been for the purpose of encouraging the Applicant to narrow the claims. While the Applicant acknowledges the duty to make the claims understandable, the Applicant respectfully submits that there is no obligation to narrow the claims, for the purpose of making the prior art search easier to perform. In fact, it might be

considered a breach of the Attorney's duty to narrow the claims, except in the face of anticipating prior art. In summary, the Applicant submits that the preambles of claims 17, 33, and 35 are not incomplete.

With respect to the relationship between "each data" and "data stream", it seems clear and evident to the Applicant that an expert in the art would understand that a data stream is composed of data. However, to advance the claims to issue, the Applicant has amended claims 17, 33, and 35 to recite "each (NRZ) data in the (NRZ) data stream".

In Section 3 of the Office Action claim 33 has been rejected under 35 U.S.C. 102(b) as anticipated by Andresen et al. ("Andresen"; US 3,670,304). This rejection is traversed as follows.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The Office Action makes repeated reference to forward error correction (FEC). The Applicant respectfully submits that claim 33 does not recite the claim element of an FEC circuit.

On page 6, the Office Action equates Andresen's Amplitude Sense and Data Gate circuit 20 with the Applicant's multi-threshold circuit. However, Andresen does not describe a circuit that provides multiple estimates in response to each data input. Andresen describes a system that includes a read head 10 to detect an analog signal. A read amplifier 12 hard-limits the received signal, to create a 2-level (high or low voltage) signal. Andresen mentions that either a high or a low threshold may be used to control AND gate 16 (col. 3, ln. 68-75), and a "zero level" threshold can be used by OR gate 18 (col. 4, ln. 1-17). The two series-connected thresholds are shown as trace "B" (line 22 of Fig. 1)

and "C" (line 44 of Fig. 1) in Fig. 2. The composite threshold is shown as signal "D" (Fig. 2) and the output on line 27 (Fig. 1) is shown as signal "E" (Fig. 2). The explanation of Fig. 2 also states that when the amplitude of the digital signal deteriorates, the system reverts back to the analog signal (col. 5. ln. 72 through col. 6, ln 8). Andresen also describes circuitry that is used to create the limiting thresholds. In short, Andresen describes a system that hard-limits analog data using a composite threshold, and uses feedback to control the limiting thresholds.

Claim 33 recites that the multi-threshold circuit outputs a plurality of bit estimates for each (input) data. Andresen shows only a single hard-limited signal for each data input (tape track), although there can be up to 9 parallel inputs (tracks), see Andresen Fig. 3. In this case, Andresen generates nine estimates, one for each of the nine inputs.

The Office Action also equates Andresen's comparators 138 and 124 in Figs. 6 and 7, with the Applicant's non-causal circuit. Andresen describes this circuitry as a Data Detector, which is block 28 of Fig. 1. The hard-limited input signal (line 28 in Fig. 1 and "A" in Fig. 6) is the input to the data detector. In the data detector (Fig. 6), the hard-limited signal is converted to narrow pulses and ANDed with the clock pulses. The result is sent to a one-shot 116, to create the data pulses "C" (Fig. 7) (col. 8, ln. 17-36).

Comparator 124 generates the clock pulse ("E" in Fig. 7) from a sawtooth, RC time constant input waveform (col. 8., ln. 37-49). Comparator 138 is used to detect phase error by monitoring waveform "D". If the "D" pulse is too long, a pulse is generated and sent to the phase error latch, block 26 of Fig. 1 (col. 9, ln. 1-23). The final clock pulse is waveform "E" (Fig. 7).

The clock pulse ("E", Fig. 7)) is fed back to AND gates 132 and 134. This ANDed output is, in turn, ANDed (118) with the data pulses ("C", Fig. 7) to generate the "1s" data waveform "G" (col. 8, ln. 61-75).

In comparing Andresen to the claimed non-causal circuit, the Office Action states that, "bit value reference decisions R1 and R2 are predetermined reference values made across a plurality of clock cycles". However, Andresen's comparators 124 and 138 generate clock pulses and phase errors, respectively. The constant amplitude voltage levels associated with R1 and R2 can be clearly seen in Fig. 7. Since R1 and R2 are merely dc voltages used to generate clock and phase information, they cannot represent "bit values determined in non-current clock cycles", as recited in the Applicant's claim.

The Office Action (page 8) states that Andresen's XOR circuit 112 receives a current bit estimate "A" and a previous bit estimate "A" from delay 110. The Office Action asserts that the output of delay 110 is a bit value from a non-current clock cycle that is being compared to a current clock cycle estimate. However, this analysis is incorrect in a number of respects. XOR 112 compares an input pulse ("A") to a delayed version of the same pulse. In this manner, narrow pulses ("B") are created that are associated with the rising and falling edges of the "A" pulses. Andresen states that, "(t)he digital signal is converted into a pulse signal for each transition by delay 110 and exclusive OR 112." (col. 8, ln. 19-21). These "B" pulses are an input in the creation of the data pulses "C". The Applicant respectfully submits that Andresen's gate delays are being confused with clocked data bits.

The claimed invention recites comparing a bit estimate for a current clock cycle to bit values determined in non-current clock cycles. As described above in the Applicant's explanation of Andresen's circuit, Andresen generates a clock ("E") from the input data. The only clocked data pulse

generated by Andresen ("G"), occurs as a result of comparing clock waveform "E" to data waveform "C". Further, this waveform "G" is only a waveform of clocked "1s" data. Nowhere does Andresen describe clocked data pulses "G" being used in the analysis of any subsequently received waveforms. Since Andresen does not show waveform "G" being compared to the subsequent input "A", he does not teach the claimed invention non-causal circuit.

It is the Applicant's position that the claims, prior to this amendment, could be clearly distinguished from the cited prior art. However, to advance the claims to issue, the claims have been amended to more clearly recite the 'first bit estimate" (as previously recited) as a "plurality of bit estimates made for the current clock cycle". The claims have also been amended to recite that the bit estimates made for the current clock cycle are compared to bit decisions made in "previous and subsequent clock cycles", as opposed to "non-current clock cycles" (as previously recited). As mentioned earlier, the Applicant Attorney feels that he has a responsibility to his client to keep the claims as broad as possible. Since the prior art reference does not include any of the Applicant's claim limitations, it is unnecessary for the Applicant to significantly narrow the claims. Alternately stated, the Applicant feels entitled to broad claims, as the claims describe a pioneering invention.

In summary, Andresen does not describe a multi-threshold circuit that outputs a plurality of bit estimates for each input data. Neither does Andresen describe a non-causal circuit that determines a current bit value in response to comparing a bit estimate to bit values determined in prior and subsequent clock cycles. Even if Andresen did describe a multi-threshold circuit and a feedback circuit that compared current bit decisions to previous bit decisions, which the Applicant strenuously denies, it is especially clear that

Andresen's feedback circuit does not make any decisions based upon subsequent (future) bit values. For this reasons alone, the invention of claim 33 can be clearly distinguished, and the Applicant requests that the rejection be removed.

In Section 4 of the Office Action claim 17 has been rejected under 35 U.S.C. 103(a) as unpatentable over Andresen in view of the IEEE dictionary definition of NRZ. The Office Action acknowledges Andresen does not teach the use of NRZ, but that it would have been obvious to modify Andresen, using the IEEE dictionary, to incorporate the use of NRZ. The Office Action states that the modification would have been obvious because one skilled in the art would have recognized the advantages of using NRZ to improve the readability of a magnetic medium. This rejection is traversed as follows.

An invention is unpatentable if the differences between it and the prior art would have been obvious at the time of the invention. As stated in MPEP § 2143, there are three requirements to establish a *prima facie* case of obviousness.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck* 947 F.2d 488, 20 USPQ2d, 1438 (Fed. Cir. 1991).

With respect to the first *prima facie* requirement to prove obviousness, the Applicant submits that the stated motivation to combine is based upon an incomplete and faulty analysis. Even if there is motivation to use an NRZ format on a tape drive system, no analysis has been performed as to how such a combination would make the claimed invention obvious.

The issue of motivation does not concern itself with whether there is some element of commonality between references. If it did, then any two references could be combined merely as the result of a common keyword. The analysis must determine if there is any motivation to modify Andresen, using NRZ, in such a manner as to teach the claimed invention. The IEEE dictionary may provide a motivation to improve a tape drive. However, the claimed invention is not simply a tape drive system. Alternately stated, even if there is a motivation to combine the NRZ definition and Andresen, the invention suggested is not the claimed invention.

With respect to the second *prima facie* obviousness requirement, even if the references are combined, there is no reasonable expectation of success. That is, even if an expert where given the Andresen tape drive enabled to use NRZ, there is no support for the assumption that an expert could derive a circuit that supplies multiple bit estimates for each input data, or a circuit that make a bit value decision based upon a comparison of a current clock cycle bit estimate, with bit values decided in prior and subsequent clock cycles.

With respect to the third *prima facie* requirement, the combination of references does not teach all the limitations of the invention of claim 17. First, the claimed invention recites a multi-threshold circuit that provides a plurality of bit estimates for each (input) data. The Applicant submits that neither Andresen nor the IEEE definition teach the generation of a plurality of bit estimates for each data input. Further, neither Andresen nor the IEEE definition describes a circuit that compares a current clock cycle estimate to bit values that were decided in prior and subsequent clock cycles. Since the combination of references does not explicitly teach all the limitations of claim 17, or suggest modifications that would make these limitations obvious, the Applicant requests that the rejection be removed.

In Section 5 of the Office Action claim 35 has been rejected under 35 U.S.C. 103(a) as unpatentable over Andresen and the IEEE dictionary definition of NRZ, in view of Abe et al. ("Abe"; US 5,781,588). The Office Action acknowledges that Andresen does not teach the use of NRZ, or the use of FEC error statistics to set a threshold, but that it would have been obvious to modify Andresen, using the IEEE dictionary and Abe. The Office Action states that the modification would have been obvious because one skilled in the art would have recognized the advantages of using NRZ to equalize BER's for different symbol states. This rejection is traversed as follows.

Abe describes 51 variations of an FSK demodulator (col. 1, ln. 35 through col. 10, ln. 39). A frequency converter converts the received signal to a second frequency, lower that the first (received) frequency. The second frequency signal is demodulated to baseband. The baseband signal is compared to a threshold, and the number of threshold crossings is counted. In the embodiment mentioned at col. 23, ln. 42-46 (Fig. 18), the baseband signal is said to be in NRZ format.

With respect to the first *prima facie* requirement to support a case of obviousness, there must be a motivation, either in the references or in the general art, to combine the references in such as way as to make the claimed invention obvious. The Office Action states that "one of ordinary skill in the art would have recognized that the use of non-return to zero NRZ would have provided the opportunity to apply the teachings in the Andresen patent to the specific type of data for which it was designed such as NRZ which is a widely used for of encoding for magnetic storage devices in order to equalize BER's for respective different symbol states (col. 36, lines 27-29 in Abe)."

However, prior art references cannot be combined for the purposes of an obviousness analysis merely on the basis of a retrospective desire to

combine different subject matter. Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion of motivation in the references to do so." *In re Mills*, 916 F.2d 680, 682, 16 USPQ2d 1430, 1432 (Fed. Cir. 1990). Here, the analysis must determine if there is any motivation in the Abe reference to modify Andresen in such way as to make the claimed invention obvious. The Applicant respectfully submits no evidence has been supplied showing that Abe, or the knowledge generally available in the art, supplies such motivation. In summary, the Applicant respectfully submits that a *prima facie* case for supporting a motivation to combine references has not been made.

With respect to the second *prima facie* obviousness requirement, even if the references are combined, there is no reasonable expectation of success. That is, even if an expert where given the Andresen and Abe inventions as a foundation, it is unlikely that they could come up with a circuit that supplies multiple bit estimates for each input data, or a circuit that make a bit value decision based upon a comparison of a current clock cycle bit estimate, with bit values decided in prior and subsequent clock cycles. No analysis has been provided to show how an expert could be expected to change Andresen's hard-limiter into a multi-threshold circuit. Neither is there any analysis of how Andresen's conventional self-clocking data circuit could be modified to use the decisions made in non-current clock cycles to influence the current clock cycle decision.

The combination of references most clearly fails to support the third *prima facie* requirement, as the combination does not teach all the limitations of the invention of claim 35. First, the claimed invention recites a multi-threshold circuit that provides a plurality of bit estimates for each (input) data. The Applicant submits that neither Andresen nor Abe generate a

plurality of bit estimates for each data input. Even if Andresen's hard-limited signal could be considered to be a bit estimate, Andresen supplies only a single "estimate" for each input (tape track). Further, neither Andresen nor Abe describes a circuit that compares a current clock cycle estimate to bit values decided in prior and subsequent clock cycles. Neither Andresen nor Abe describe an FEC circuit that generates the threshold levels used by the multi-threshold circuit.

The affidavit of George Bendak is enclosed herein as attachment A, to support the Applicant's position. The affidavit was prepared to rebut the obviousness rejections made by the Examiner, and to bolster the Applicant's description of the prior art, which is at odds with arguments presented in the Office Action. Mr. Bendak's description of the Andresen and Abe patents generally supports the Applicant's explanations, and disagrees with the descriptions presented in the Office Action. It is Mr. Bendak's opinion that the Andresen reference does not include any of the claim limitations recited in claims 17, 33, or 35. It is also Mr. Bendak's opinion that even if the all the prior art references were combined, that combination neither explicitly describes the Applicant's base claims, nor suggests a modification that would make the base claims obvious.

It is believed that this application is now in a condition of allowance.

Respectfully submitted,

Date: 8/4/2005

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